REMARKS

This application is believed to be in condition for allowance at the time of the next Official Action.

The Official Action rejects claims 1, 10, 19, and 22 under 35 USC §103(a) as being unpatentable over GÖTZE et al. in view of CARLTON et al. Reconsideration and withdrawal of this rejection are respectfully requested for the following reasons:

Of the rejected claims, claims 1 and 10 are independent, with the former directed to an apparatus, and the latter directed to a method. Whether recited in the form of apparatus or method, each claim requires the following in the specified sequence:

- an interface receives a parallel data bus that is *m* bits wide as an input, and converts the *m* bit wide data into sequentially generated *n* bit wide parallel data segments, with $n < m$;

- the *n* bit wide parallel data segments are then received as an input and used to generate an error correcting code, with the error correcting code added in parallel to each *n* bit wide parallel data segment; and

- each of the *n* bit wide parallel data segments with the associated error correcting code are then received as an input and converted into serial data.

Given the nature of the recitations in both the apparatus and method claims, the sequence, must be as listed

above. Accordingly, any combination of references must suggest, in their totality, not only each individual structural element or method step, but also the sequential interrelationship therebetween.

The Official Action freely acknowledges that the GÖTZE reference fails to offer any teaching whatsoever of receiving an *m* bit wide parallel bus and multiplexing the same into sequentially generated *n* bit wide parallel data segments. The Official Action overcomes this failing by taking official notice that is well known in the art of communications to use multiplexers and demultiplexers to convert data streamed on one size bus to data streamed on a different size bus. The Official Action then goes on to say that it would have been obvious to one of ordinary skill in the art at the time of the invention to include a multiplexer and demultiplexer into the system of GÖTZE et al. The stated motivation for this modification of the GÖTZE et al. device is that multiplexers and demultiplexers are simple logic devices that make this system more dynamic by allowing the use of different size buses, which in turn is offered as enabling components operating at different speeds to work together.

At the outset, applicant would greatly appreciate an expansion of the explanation of the interrelationship between different widths of parallel data buses and operating speeds.

Applicant also solicits a further explanation of the meaning of "different size buses can be used." If the intended

meaning of this stated motivation is that the input width of a multiplexer or demultiplexer is different from the output bus width, applicant respectfully suggests that the assertion is accurate but without meaning. Multiplexers and demultiplexers have different width input and output buses because that is what multiplexers and demultiplexers do. The fact of the existence of multiplexers and demultiplexers is not in itself any particular motivation to utilize such devices.

As to the requirement in each claim of a parallel-to-serial conversion of the *n* bit wide parallel data segments with the added error correcting code into serial data, the Official Action acknowledges that the primary reference fails to offer any such suggestion. The Official Action therefore relies on the secondary CARLTON et al. reference.

Irrespective of the ability of the CARLTON et al. reference to suggest the particular feature of converting parallel data with an added error correcting code into serial data, as yet unanswered is the question of why one of skill in the art would further modify the modified GÖTZE device at all. Beyond this, it is unclear why one would undertake the steps or implement the structure of the present rejected claims, each of which specifically requires the sequential components of taking a first parallel bus and dividing it into sequentially generated but nevertheless parallel data segments of smaller width, and only after such first parallel-to-parallel conversion,

implementing a subsequent parallel-to-serial conversion. If one were to treat the primary reference as teaching the generation of ECC bits for parallel data, and the second reference as converting parallel data with error correction information into serial data, the reasonable combination that would flow from these teachings would be the single-step conversion of parallel-to-serial data, not the two-step approach of parallel-to-parallel conversion followed by parallel-to-serial conversion of the present invention as recited in the rejected claims.

As the overall combination of references fails to fairly teach or suggest the features recited in independent claims 1 and 10, applicant respectfully suggests that the present obviousness rejection cannot reasonably be maintained.

The Official Action rejects claims 3, 4, 12, 13, 15, 17, 20, 23, 24, and 26 under 35 USC §103(a) as being unpatentable over RUB. The Official Action separately rejects claims 5, 14, and 18 as unpatentable over RUB in view of GÖTZE et al. Reconsideration and withdrawal of both rejections are respectfully requested for the following reasons:

The applied reference is a U.S. patent issued October 12, 2004. The application underlying such patent first published December 27, 2001. The RUB reference makes no priority claim to a foreign application which might have an earlier publication date. Given the U.S. filing date of October 11, 2001 for the present application, neither the RUB patent or any known

earlier publication of the content of such patent constitutes 102(b) prior art against the present application.

The application underlying the RUB patent was filed June 26, 2001. Such filing date renders the RUB patent as 102(e) prior art only if the present applicant cannot prove a date of invention prior to such filing date. To this end, applicant includes herewith a verified translation of the Japanese application filed October 11, 2000, the priority of which is claimed by the present application. This conclusively proves a date of constructive reduction to practice prior to the June 26, 2001 filing date of the RUB application.

The RUB application makes a claim to the priority of a provisional application filed June 27, 2000. Under current U.S. practice, the filing date of such a provisional application is considered to be the 102(e) date of the U.S. patent as a reference, but only if and to the extent that the provisional application supports the disclosure of the subsequently filed regular application.

Accordingly, applicant includes herewith a full copy of Provisional Application No. 60/214,699, which underlies the RUB patent. As is clear from a review of such filing, the provisional application amounts to little more than a set of Powerpoint slides presented at the level of an executive summary. As such, the provisional application discloses none of the disclosure for which the RUB et al. patent is offered.

As the provisional application itself would not support the present rejection, the earliest 102(e) date attributable to the applied reference is its regular application filing date. In light of the demonstrated date of earlier constructive reduction to practice provided by the enclosed verified translation, the applied reference is not prior art with respect to the rejection claims, and the rejections necessarily fail.

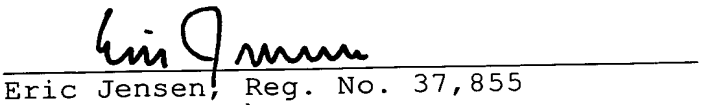
In light of the analysis provided above, applicant believes the present application is in condition for allowance, and an early indication of the same is respectfully requested.

If the Examiner has any questions or requires further clarification of any of the above points, the Examiner may contact the undersigned attorney so that this application may continue to be expeditiously advanced.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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APPENDIX:

- verified translation of the Japanese priority application
- full copy of Provisional Application No. 60/214,699

JUN 29 2006
PATENT & TRADEMARK OFFICE
IAP90

jc406 U.S. PTO
60/214699
06/27/00

jc860 U.S. PTO
06/27/00

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PTO/SB/16 (2-98)
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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

INVENTOR(S)		
Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Bernardo	Rub	Edina, MN

☐ *Additional inventors are being named on the __ separately numbered sheets attached hereto*

TITLE OF THE INVENTION (280 characters max)

CODING WITH UNEQUAL PROTECTION FOR MAGNETIC RECORDING CHANNELS WITH CONCATENATED ERROR CORRECTING CODES

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

☐ Customer Number [ ] → *Place Customer Number Bar Code Label here*

OR *Type Customer Number here*

☒ Firm or Individual Name	Seagate Technology, Inc.				
Address	Intellectual Property – SHK2LG				
Address	1280 Disc Drive				
City	Shakopee	State	MN	ZIP	55379-1863
Country	USA	Telephone	952-402-2517	Fax	952-402-2657

ENCLOSED APPLICATION PARTS (check all that apply)

☒ Specification *Number of Pages* 12 ☐ Small Entity Statement

☐ Drawing(s) *Number of Sheets* [ ] ☒ Other (specify) Return Receipt Postcard

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT *(check one)*

☐ A check or money order is enclosed to cover the filing fees

☒ The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number: 19-1038

FILING FEE AMOUNT ($): 150.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are: _____

Respectfully submitted,

SIGNATURE _____ Date 6/27/00

TYPED or PRINTED NAME Shawn B. Dempster

REGISTRATION NO. *(if appropriate)* 34,321

TELEPHONE 952-402-2517

Docket Number: SEA9712.01

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is used by the public to file (and by the PTO to process) a provisional application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the complete provisional application to the PTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C., 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Box Provisional Application, Assistant Commissioner for Patents, Washington, D.C. 20231.

OIPE IAP90 JUN 29 2006 PATENT & TRADEMARK OFFICE

Attachments to Coding IP disclosures
B. Rub
6/19/2000

Three inventions described in the attached Powerpoint presentation "Coding 2000-06-15" are summarized below. These are being submitted as three separate inventions with a broad scope. As the work proceeds, subsequent inventions for detailed implementations are expected.

Coding with unequal protection for magnetic recording channels with concatenated error correcting codes

- Concept for matching channel code design to ECC with the intent of providing greater protection against channel error events that have a greater impact on the ECC
- For magnetic recording channels concatenated with a Reed-Solomon ECC, the channel code is designed to provide greater protection against errors that span ECC symbol boundaries.
- It is common practice to target specific error event types. What is being proposed is to target error events at specific locations, namely those most likely to result in errors in two consecutive ECC symbols.
- A code, called Boundary MTR code, for removing tribit error events at ECC symbol boundaries is proposed. The code eliminates two NRZ patterns or one NRZI pattern that results in a tribit with the middle transition at the ECC symbol boundary. Eliminating these patterns and imposing the corresponding constraints on the detector remove the two possible tribit error events at the symbol boundaries or any larger error events that include tribits at the boundaries.

Symbol Level coding for magnetic read channel concatenated with error correcting codes

- Method for approximating the benefits of having a single bit of parity for each ECC symbol but with a much lower code rate loss
- Effectively targets single occurrences of error events with an odd number of ones (odd parity) which are the most frequent errors in magnetic recording channels.
- A method for enforcing code constraints at a symbol level is described and a procedure for inserting appropriate parity bits at the bit level so that the symbol level constraints are satisfied.

Coding system for magnetic recording channels with concatenated error correcting codes

- A coding system design that includes the following constraints:
  1. A boundary MTR constraint that is enforced in the Trellis of a Viterbi detector or in a postprocessor with equivalent functionality.
  2. A symbol level code that imposes constraints on a symbol level sequence derived by generating a bit from each ECC symbol.
  3. A bit level code to target error events not removed by either the boundary MTR or the symbol level codes.
  4. A symbol based error correcting code such as a Reed-Solomon Code.

Coding for Magnetic Recording Channels
6/15/2000

Matched Coding

- Coding considerations for disc drive applications
  - Matched to ECC characteristics
    - Correction units is one symbol
  - Matched to channel error characteristics
    - Predominantly odd-length error events

Matching to ECC Characteristics

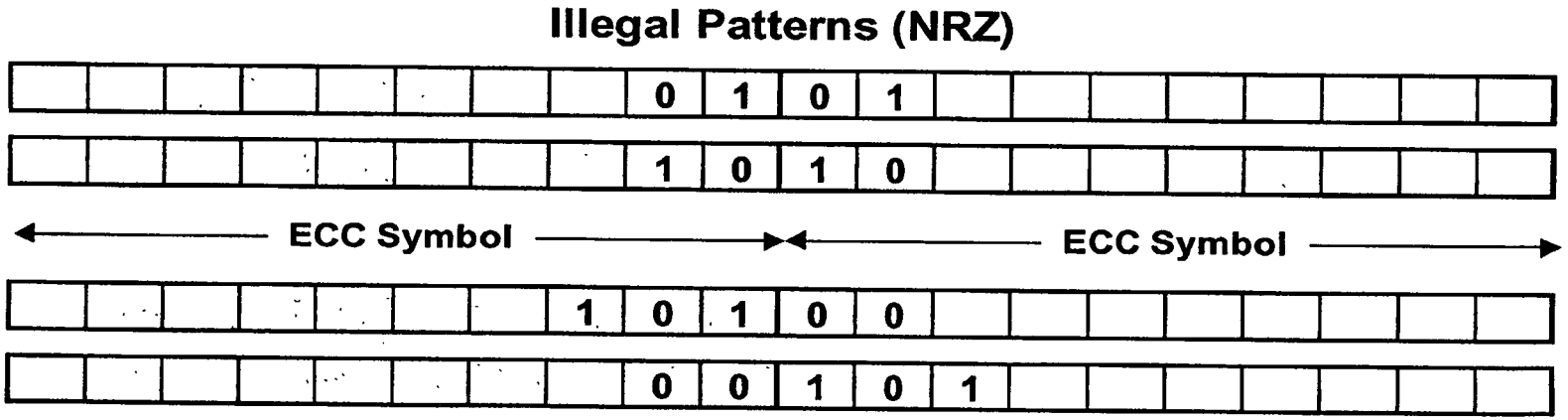
- ECC unit is one symbol (not one bit)
- Not all bit errors have the same impact
- For example,
  - a 10 bit error within a single 10 bit ECC symbols -> 1 symbol error
  - 1 2 bit error across symbol boundary -> 2 symbol error
- Therefore,
  - it is more important to minimize errors across ECC symbol boundaries than to minimize errors within an ECC symbol
- Proposed consideration for channel coding
  - Have unequal bit error rate probabilities
    - lower at boundaries, higher within ECC symbol
  - Design code to have more protection for boundary bits

Trellis Coding

- We can use trellis coding to remove most error events that result in two ECC symbol errors
- With magnetic recording channels, most likely error events are one bit or three bits.
  - One bit errors always result in a one bit ECC symbol error
  - A three bit error can result in 2 ECC symbol errors
- MTR constraint
  - MTR codes were proposed to eliminate all Tribit errors
    - Disadvantage is large code rate penalty
  - Efficient compromise
    - Eliminate all tri bit errors at ECC symbol boundaries
- Variation for any code constraint to eliminate likely error events
  - Increase rate by eliminating errors at boundaries only

Boundary MTR Code

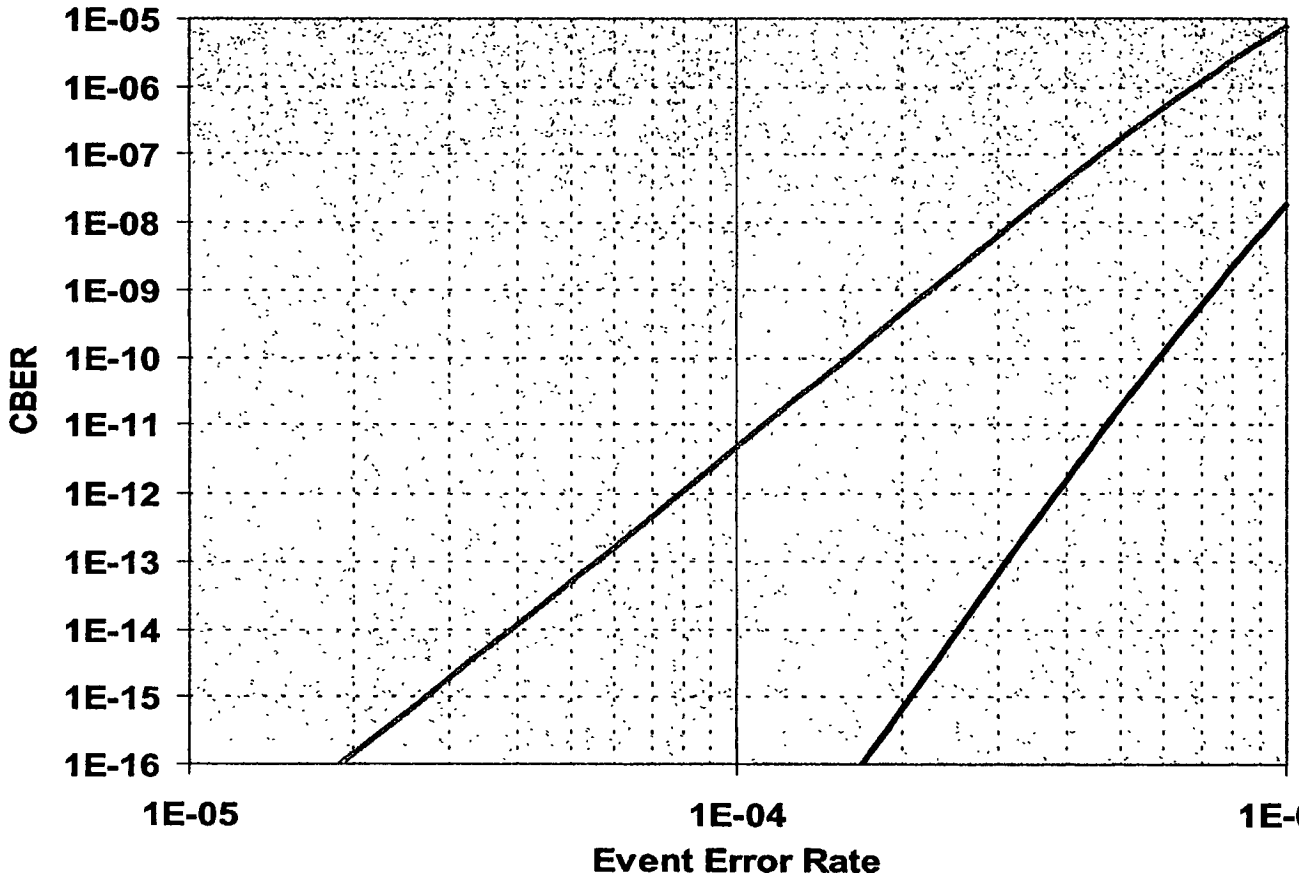
Can be implemented with a rate of 39/40 (.975)



Errors in a sector

- Min. Distance Argument
  - What is the minimum number of error events in a sector that is uncorrectable?
- Example
  - Assume channel only has 3 bit errors
  - Assume ECC with T=12, I=1, 10 bit symbols
  - With no coding:
    - It takes 7 error events in a sector to exceed the ECC capability
  - With 1 bit parity
    - It takes 8 error events in a sector to exceed the ECC capability
      - Errors come in pairs
  - 1 bit parity does not help much to increase the minimum distance at sector level
  - With boundary MTR code and no parity
    - It takes 13 error events in a sector to exceed the ECC capability
  - Which of the scenarios above would work better?

Coding with unequal protection



Effect of Elimninating Boundary Errors

- Example with only 4 bit error events
- ECC: T=12, I=1, 10 bit symbols

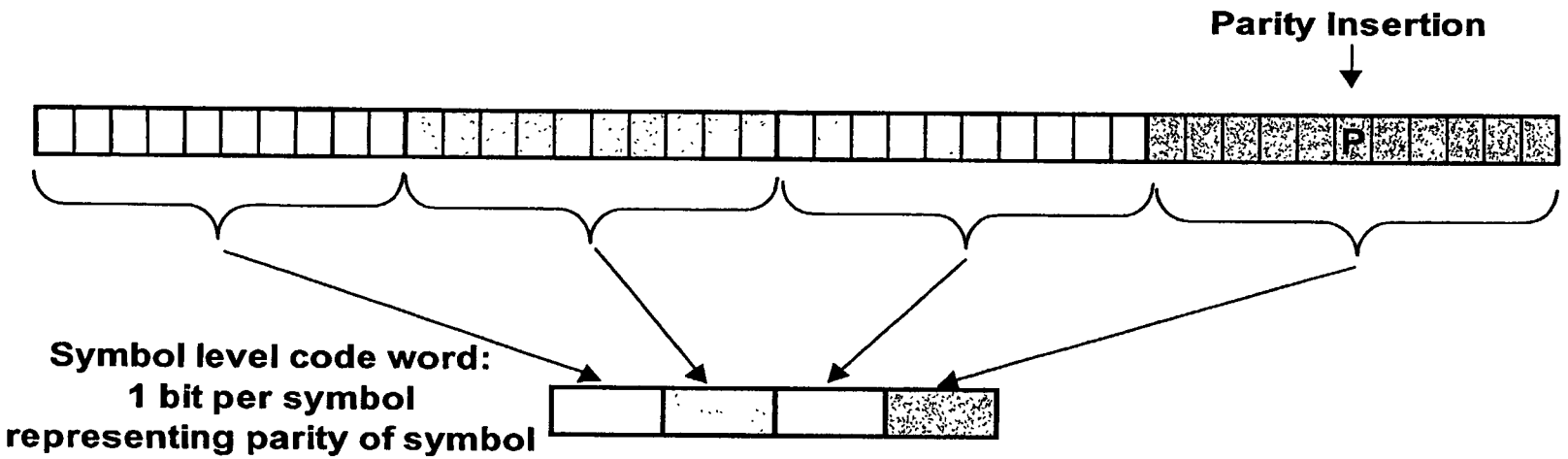
Uncoded
Boundary MTR

-8-

Removing most likely error events

- Most likely error events
  - Odd error events
    - 1 bit, tribit
- Proposed approach to correct most odd error events
  - apply code constraints at symbol level

Symbol Level Code



Example: single bit symbol level parity
1 bit is added to guarantee even or odd symbol level parity

- Coding in three levels
  - Trellis code to eliminate error events that include tribit at symbol boundary
  - Symbol level code to protect against errors with odd symbol parity
  - Bit level coding to protect against remaining errors

Examples

Code Word Size (bits)	Trellis Code	Symbol Level Code	Bit Level Code	Code Rate
165	4 x 39/40	16,11 (dmin=4)	-	0.94545
326	8 x 39/40	32,26 (dmin=4)	-	0.95706
330	8 x 39/40	32,22 (dmin=6)	-	0.94545
335	8 x 39/40	32,17 (dmin=8)	-	0.93134
652	16 x 39/40	64,52 (dmin=6)	-	0.95706
657	16 x 39/40	64,47 (dmin=8)	-	0.94977
657	16 x39/40	64,57 (dmin=4)	permuter + 10-bit parity	0.94977
662	16 x39/40	64,52 (dmin=6)	permuter + 10-bit parity	0.9426
4560	110 x 39/40	440,280 (LDPC?)	-	0.93487
4560	110 x 39/40	440,340 (LDPC?)	4560,4480 ???	0.93487

-12-